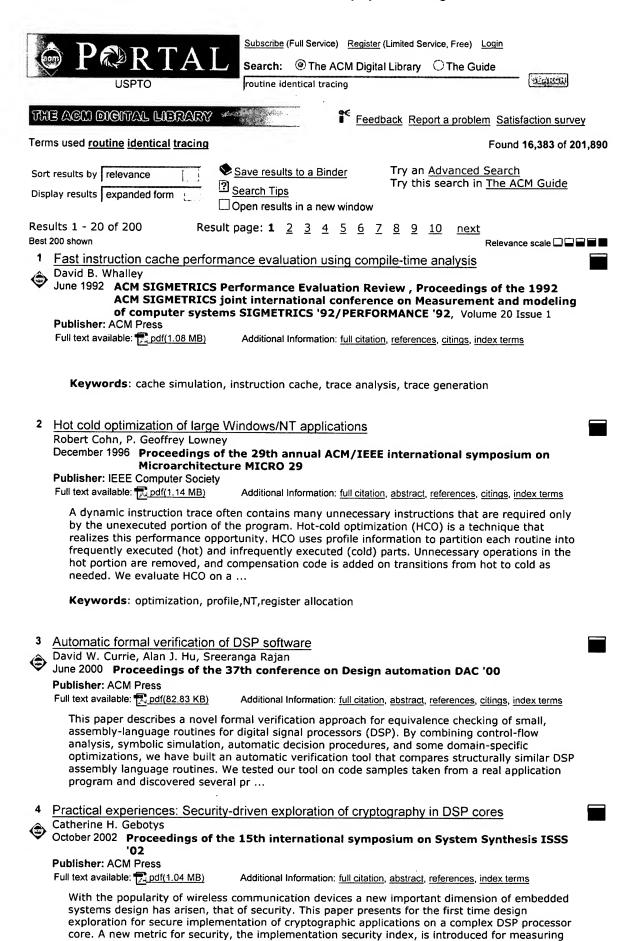


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resistance to power attacks. Elliptic curve cryptographic algorithms are used to demonstrate and

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Adding trace matching with free variables to AspectJ Chris Allan, Pavel Avgustinov, Aske Simon Christensen, Laurie Hendren, Sascha Kuzins, Ondřej Lhoták, Oege de Moor, Damien Sereni, Ganesh Sittampalam, Julian Tibble October 2005 ACM SIGPLAN Notices, Proceedings of the 20th annual ACM SIGPLAN conference on Object oriented programming, systems, languages, and applications OOPSLA '05, Volume 40 Issue 10 Publisher: ACM Press
Full text available: pdf(392.31 KB) Additional Information: full citation, abstract, references, citings, index terms
An aspect observes the execution of a base program; when certain actions occur, the aspect runs some extra code of its own. In the AspectJ language, the observations that an aspect can make are confined to the <i>current</i> action: it is not possible to directly observe the <i>history</i> of a computation. Recently, there have been several interesting proposals for new history-based language features, most notably by Douence <i>et al.</i> and by Walker and Viggers. In this paper, we present a ne
Keywords: aspect-oriented programming, program monitoring
A dynamic multithreading processor Haitham Akkary, Michael A. Driscoll November 1998 Proceedings of the 31st annual ACM/IEEE international symposium on Microarchitecture MICRO 31 Publisher: IEEE Computer Society Press Full text available: pdf(2.67 MB) Additional Information: full citation, references, citings, index terms
Instruction fetch and control flow: Power-efficient instruction delivery through trace reuse Chengmo Yang, Alex Orailoglu September 2006 Proceedings of the 15th international conference on Parallel architectures and compilation techniques PACT '06 Publisher: ACM Press Full text available: pdf(260.98 KB) Additional Information: full citation, abstract, references, index terms As power dissipation inexorably becomes the major bottleneck in system integration and reliability, the front-end instruction delivery path in a traditional out-of-order superscalar processor needs to deliver high application performance in an energy-effective manner. This challenge can be addressed by efficiently reusing the work of fetch and decode performed during preceding loop iterations and resident mostly within the processor itself. As a large percentage of the instructions currently und Keywords: adaptive processor, instruction delivery, low-power design
traction delivery, low power design
Integration and applications of the TAU performance system in parallel Java environments Sameer Shende, Allen D. Malony June 2001 Proceedings of the 2001 joint ACM-ISCOPE conference on Java Grande JGI '01 Publisher: ACM Press
Full text available: pdf(2.17 MB) Additional Information: full citation, abstract, references, citings, index terms
Parallel Java environments present challenging problems for performance tools because of Java's rich language system and its multi-level execution platform combined with the integration of native-code application libraries and parallel runtime software. In addition to the desire to provide

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